AMENDMENTS

In the Claims:

Please amend claims as follows.

Claims 1-6 (canceled).

Claim 7 (previously cancelled).

Claims 8-12 (canceled).

13. (original) A method for fabricating a nitride read-only memory, comprising:

forming a silicon oxide/silicon nitride/silicon oxide (ONO) stacked layer on a substrate, the ONO stacked layer consisting of a bottom oxide layer, a silicon nitride layer and a top oxide layer;

forming a protective layer on the ONO stacked layer, the protective layer having a thickness smaller than 50Å;

patterning the protective layer and the ONO stacked layer to form a plurality of stacked patterns, wherein an etching rate of the protective layer is lower than an etching rate of the top oxide layer;

performing an ion implantation to form a plurality of buried bit lines in the substrate between the stacked patterns;

forming an insulator on each buried bit line; and

forming a plurality of word lines on the substrate.

14. (original) The method of claim 13, wherein a thickness of the bottom oxide layer is about 50~100Å.

15. (original) The method of claim 13, wherein a thickness of the silicon nitride layer is about 55~80Å.

16. (original) The method of claim 13, wherein a thickness of the top oxide layer is about 70~120Å.

17. (currently amended) The method of claim 13, wherein the protective layer comprises silicon nitride.

18. (currently amended) The method of claim 13, wherein the insulator comprises silicon oxide.

19. (original) The method of claim 13, wherein the word lines comprise polysilicon.

20. (original) The method of claim 13, wherein the ONO stacked layer is patterned until a portion of the bottom oxide layer is exposed.

21. (original) The method of claim 20, wherein the exposed bottom oxide layer is removed after the ion implantation is performed.

22. (previously presented) The method of claim 1, wherein a thickness of the protective layer is smaller than 50Å.

23. (new) A method for fabricating a nitride read-only memory, comprising:

forming a silicon oxide/silicon nitride/silicon oxide (ONO) stacked layer on a substrate, the ONO stacked layer consisting of a bottom oxide layer, a silicon nitride layer and a top oxide layer;

forming a protective layer on the ONO stacked layer, wherein a thickness of the protective layer is smaller than 50Å;

patterning the protective layer and the ONO stacked layer to form a plurality of stacked patterns, wherein an etching rate of the protective layer is lower than an etching rate of the top oxide layer so that the protective layer protects the top oxide of the ONO stacked layer during the patterning step; and

removing the protective layer.

24. (new) The method of claim 23, wherein a thickness of the bottom oxide layer is about 50~100Å.

25. (new) The method of claim 23, wherein a thickness of the silicon nitride layer is about 55~80Å.

26. (new) The method of claim 23, wherein a thickness of the top oxide layer is about 70~120Å.

27. (new) The method of claim 23, the protective layer comprises silicon nitride.

28. (new) The method of claim 23, further comprising:

performing an ion implantation to form a plurality of buried bit lines in the substrate between the stacked patterns;

forming an insulator on each buried bit line; and

forming a plurality of word lines on the substrate.

29. (new) The method of claim 28, wherein the insulator comprises silicon oxide.

30. (new) The method of claim 28, wherein the word lines comprise polysilicon.

31. (new) The method of claim 23, wherein the ONO stacked layer is patterned until a portion of the bottom oxide layer is exposed.

32. (new) The method of claim 31, wherein the exposed bottom oxide layer is removed after the ion implantation is performed.